CLAIMS

1. A DDR apparatus comprising:

a pattern generating device to generate a clock test pattern and a data test pattern; and

buffer devices to receive said clock test pattern and said data test pattern;

a pattern checking device to check patterns received from said buffer devices; and

clock generating logic to control a clock for said clock test pattern and a clock for said data test pattern.

2. The DDR apparatus of claim 1, wherein said clock generating logic operates such that in a test mode the clock for the clock test pattern is in phase with said clock for said data test pattern.

3. The DDR apparatus of claim 2, wherein said test mode comprises an AC I/O loopback test.

4. The DDR apparatus of claim 1, wherein said clock generating logic operates such that in a normal mode, said clock for said clock test pattern is out-of-phase with said clock for said data test pattern.

5. The DDR apparatus of claim 1, wherein said buffer devices are provided within a memory controller.

6. The DDR apparatus of claim 1, wherein said clock generating logic includes a delay element.

7. The DDR apparatus of claim 1, wherein said clock generating logic includes at least one switching element to switch among a plurality of different modes.

8. The DDR apparatus of claim 7, wherein said clock generating logic further includes state logic to control signals applied to said at least one switching element.

9. A circuit comprising:

a pattern generating device to generate a clock test pattern and a data test pattern for at least one DDR I/O cell;

a pattern checking device to check patterns passing through said at least one DDR I/O cell; and

clock generating logic to control a clock for said clock test pattern and a clock for said data test pattern.

10. The circuit of claim 9, wherein said clock generating logic operates such that in a test mode the clock for the clock test pattern is in phase with said clock for said data test pattern.

11. The circuit of claim 9, wherein said test mode comprises an AC I/O loopback test mode.

12. The circuit of claim 9, wherein said clock generating logic operates such that in a normal mode, said clock for said clock test pattern is out-of-phase with said clock for said data test pattern.

13. The circuit of claim 9, wherein said at least one DDR I/O cells is provided within a memory controller.

14. The circuit of claim 9, wherein said clock generating logic includes a delay element.

15. The circuit of claim 9, wherein said clock generating logic includes at least one switching element to switch among a plurality of different modes.

16. The circuit of claim 15, wherein said clock generating logic further includes state logic to control signals applied to said switching element.

17. A clock generating circuit to generate a first clock signal and a second clock signal for a DDR device, wherein said clock generating circuit generates said first clock signal in phase with said second clock signal when in a test mode and generates said first clock signal out of phase with said second clock signal when in a normal mode.

18. The clock generating circuit of claim 17, wherein said test mode comprises an AC I/O loopback test.

19. The clock generating circuit of claim 17, wherein said DDR device is provided within a memory controller.

20. The clock generating circuit of claim 17, wherein said clock generating logic includes a delay element.

21. The clock generating circuit of claim 17, wherein said clock generating logic includes at least one switching element to switch between at least said test mode and said normal mode.

22. The clock generating circuit of claim 23, wherein said clock generation logic further includes state logic to control signals applied to said switching element.

23. A method comprising:

generating a clock test pattern and a data test pattern;

passing said clock test pattern and said data test pattern through at least one DDR device;

checking patterns passing through said at least one DDR device; and

adjusting one of a clock for said clock test pattern and a clock for said data test pattern.

24. The method of claim 23, wherein said adjusting comprises providing said clock for said clock test pattern in phase with said clock for said data test pattern in a test mode.

25. The method of claim 24, wherein said test mode comprises an AC I/O loopback test.

26. The method of claim 23, wherein said adjusting comprises providing said clock for said clock test pattern out-of-phase with said clock for said data test pattern in a normal mode.

27. The method of claim 23, wherein said adjusting comprises using at least one switching element to switch among a plurality of modes.

28. The method of claim 27, wherein said adjusting further comprises switching in a delay element based on one of said plurality of modes.